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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/190,618	11/12/98	ZHANG H	0756-1881

MM91/1003

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EXAMINER	
LEE, E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 10/03/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/190,618	ZHANG ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *12 November 1998* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 1998* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☒ received in Application No. (Series Code / Serial Number) *08/312,795* .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

IDS

The foreign patents and non-patent publications cited in the Information Disclosure Statement were not considered in this Office Action since they were not provided by the applicant and were not in the file wrapper of the parent application. Please provide these documents in the next correspondence with the USPTO so they may be considered appropriately in the application.

Drawings

1. Figure 4A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. On page 1, paragraph 3, the applications states that figure 4A is a cross-sectional view of a *conventional* TFT. See MPEP § 608.02(g).

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 5, 10, 15, 23, and 30, the multi-layered structure of the gate electrode with the listed metals must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. The drawings are objected to because the label "FTT3" in figure 8B is incorrect. Correction is required.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: element ya', first mentioned on page 17, line 20. Correction is required.

Specification

5. The disclosure is objected to because of the following informalities: first appearing on page 5, line 10, the word "effected" should be changed to "affected"; page 6, line 28, there is a clerical error ("med"); on page 17, line 31, the word "Example" should not be capitalized;

Appropriate corrections to these and all other clerical errors are required.

Claim Objections

6. Claim 17 is objected to because of the following informalities: the word "pair" is spelled incorrectly. Appropriate correction is required.

7. Claim 20 is objected to because of the following informalities: the word "crystal" should be "crystalline." Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 19 recites the limitation "second thin film transistor" in line 13. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 1 thru 36 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 thru 18 of U.S. Patent No. 5,962,872. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the patented invention and the present claims are directed towards an active matrix circuit and a driving circuit. Each circuit contains thin film transistors that consist of regions possessing different amounts of impurity, thereby affecting the resistance of the regions. The present claims are not identical to the claims of Patent No. 5,962,872 because the patent claims refer to an electro-optical display device whereas the present claims refer to a semiconductor device. Since the present claims are generic to the more specific claims of Patent No. 5,962,872, the present claims of the application are anticipated by the '872 patent claims.

a. Regarding claims 2, 7, 12, 20, 27, the patent claims, being directed to an SOI structure, do not recite the substrate as crystalline silicon. Nonetheless it would have been obvious to one of ordinary skill in the art at the time of invention to form the insulated TFT structure on a crystalline silicon substrate to enable further integration with other types of circuits.

b. Regarding claims 3, 8, 13, 21, 28, the patent claims do not recite the phosphorus or boron as the impurity in the regions but it is well known in the art

that these two elements are commonly used to dope regions of a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use phosphorus or boron in these regions for their conventional purposes.

c. Regarding claims 4, 9, 14, 22, 29, the patent claims do not recite the gate electrode over the semiconductor film but it is well known in the art that in thin film transistors the gate electrode is necessarily either over or under the semiconductor film. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate electrode over the semiconductor film.

d. Regarding claims 5, 10, 15, 23, 30, the patent claims do not recite the gate electrode as having a multi-layered structure consisting of aluminum, tantalum, titanium or silicon. However, Dohjo et al. '551 teaches that the gate electrode may contain multiple layers that consist of, for example, tantalum. See, for example, figure 7. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a multi-layered structure gate electrode in order to improve the resistivity of the gate electrode as taught by Dohjo et al. (see, for example, column 9, line 43 and Table on columns 5 and 6).

e. Regarding claim 16, the patent claims do not recite the driving circuit as having an inverter circuit comprising of at least a second and third thin film transistors formed over a substrate. However, Shimada et al. '801 disclose that two thin film transistors form an inverter circuit that drives a liquid crystal display. See,

for example, page 1. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to know that thin film transistors are routinely used to form inverter circuits, which reside inside liquid crystal display devices.

f. Regarding claim 24, 25, 34, 35, 36, the patent claims do not recite the ranges of the concentration of impurity in the first and second regions but it is well known in the art that the recited concentration ranges are commonly used to dope low and high resistance regions in semiconductor devices. For example, see column 6, line 65 of U.S. Patent No. 5,962,872 where it states the impurity concentration. It would have been obvious to one of ordinary skill in the art at the time of invention to utilize concentrations within these conventional ranges.

g. Regarding claim 6, 11, 17, 18, 31, 32 the specific distance between the first regions and channel regions does not provide any critical or unexpected results to the TFT's operation. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mahshid Saadat can be reached on 703-308-4915. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
September 28, 2000

Mahshid Saadat
Supervisory Patent Examiner
Technology Center 2800